MODEL-EXTRAPOLATED S-PARAMETER DESIGN OF MM-WAVE GaAs FET AMPLIFIERS

Lon Dearden*, Dr. Gayle Miner**, Dr. Mohamed Sayed*

* Hewlett-Packard 1400 Fountain Grove Parkway, Santa Rosa, CA 95401
** Department of Electrical Engineering, Brigham Young University, Provo, UT 84602

ABSTRACT

Broadband millimeter-wave GaAs MESFET amplifiers have been designed from model-extrapolated S-parameters. An equivalent circuit MESFET model valid to 40 GHz is given. Amplifier performance from 15-50 GHz is shown and compared with the equivalent circuit model.

INTRODUCTION

The development of the sub-half micron GaAs MESFET in the past few years has generated greater interest in millimeter-wave FET amplifiers (1,2,3,4). Due to the difficulty of measuring device S-parameters at millimeter-wave frequencies, most FET amplifier designs above 26.5 GHz have employed an extrapolated S-parameter approach using the device equivalent circuit model.

Extrapolated S-parameters are determined by developing an equivalent circuit model whose S-parameters match those over the measured frequency band, and then, using the model to find the S-parameters at higher frequencies. Using this technique, J. Rosenberg et al. (1) demonstrated minimum gains of 5 dB for a single ended output one stage amplifier from 26.5-40 GHz and later (3) produced a single-stage balanced amplifier with 8 dB of gain over the same frequency range. E. T. Watkins et al. (4) demonstrated a one-stage amplifier with 5.5 +/- 0.5 dB of gain from 55 to 62 GHz. These previous reports (1,3,4) however, have not shown predicted performance. We present herein a methodology for designing millimeter-wave FET amplifiers on microstrip using device extrapolated S-parameters and give results for both measured and modeled performances.

DEVICE SELECTION AND MEASUREMENT

Four commercially available sub-half micron GaAs MESFET devices from three different manufacturers were selected for measurement and modeling. Some of their electrical specifications and gate dimensions from the manufacturer data sheets are presented in Table 1.

The S-parameters of the selected FETs were measured from 1.5-26.5 GHz on the HP 8510 vector network analyzer using an in-house device test fixture. Calibration standards (short, open, and load), that could be slid in and out of the test fixture, were used to calibrate out the fixture effects and to define the measurement reference planes. The gate and drain bonding meshes were included in the measured S-parameters. The measurements were taken at the bias levels indicated in Table 1. Devices #2 and #3 with lower Idss were measured at Ids=10 mA, and devices #1 and #4 were measured at Ids=30 mA for S-parameter comparison at equivalent bias conditions.

TABLE 1

Comparison of device gate dimensions and electrical performances

	MANUFACTURER DATA SHEET			MEASURED		MODELED PERFORMANCE		
DEVICE	GATE LENGTH	GATE WIDTH	TYPICAL GAIN	IDSS mA	Ids BIAS Vd=3V	F_{MAX} MODEL	G_{TU} 30 GHz	G_{TU} 40 GHz
#1	0.3μm	280μm	8.5 @ 18 GHz	65	30 mA	77 GHz	6.0dB	4.1dB
#2	0.3μm	200μm	9.9 @ 18 GHz	17	10 mA	77 GHz	6.3dB	4.5dB
#3	0.3μm	200μm	10.5 @ 12 GHz	15	10 mA	81 GHz	6.3dB	4.5dB
#4	0.25μm	200μm	8.5 @ 18 GHz	35	30 mA	85 GHz	9.0dB	6.0dB

DEVICE MODELING

The complete equivalent circuit for the device including the measurement environment is shown in Figure 1. Unlike earlier reported MESFET models (5,6), the drain-to-source capacitance is broken up into two parts. The major part of the capacitance Cds is located directly across the output resistance Rds while a smaller part Cds' is across the drain-to-source bonding pads. This was necessary to more accurately model S12 over the measured frequency range. The transadmittance was modeled as a magnitude gm and a time delay td. The gate and drain bonding meshes were modeled as high impedance transmission lines with the source mesh being lumped into an equivalent inductance.

0149-645X/86/0000-0385$01.00 © 1986 IEEE

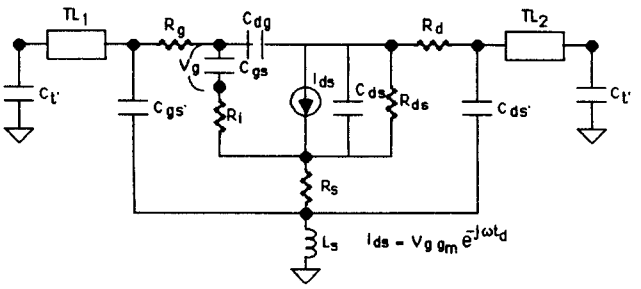

FIGURE 1

MESFET equivalent circuit including bonding meshes and associated parasitics

Initial values for the model elements were found from the 1.5 GHz scattering parameters and DC measurements. The element values were then optimized to achieve the best match between the measured S-parameters and those of the model from 1.5-26.5 GHz. The optimized element values for the four device models are shown on Table 2. The bonding meshes were removed from the models and the extrapolated performance of the devices examined. The model for device #4 indicated 1.5 dB higher unilateral gain at 40 GHz than the other devices (see Table 1). This device was used in the amplifier designs. Figure 2 shows the measured and optimized model S-parameters of device #4.

TABLE 2

Optimized equivalent circuit parameters of four MESFET devices

PARAMETER	DEVICE #1	DEVICE #2	DEVICE #3	DEVICE #4
R_g	1.7 Ω	1.6 Ω	1.5 Ω	1.8 Ω
C_{gs}	0.31 pF	0.19 pF	0.22 pF	0.24 pF
$C_{gs'}$	0.016 pF	0.02 pF	0.02 pF	0.01 pF
R_i	0.71 Ω	0.21 Ω	0.2 Ω	1.1 Ω
R_s	0.8 Ω	1.7 Ω	2.5 Ω	6.0 Ω
R_{ds}	170 Ω	320 Ω	230 Ω	310 Ω
R_d	1.1 Ω	2.1 Ω	2.5 Ω	1.4 Ω
C_{ds}	0.085 pF	0.071 pF	0.055 pF	0.055 pF
$C_{ds'}$	0.011 pF	0.015 pF	0.021 pF	0.011 pF
C_{dg}	0.035 pF	0.03 pF	0.031 pF	0.012 pF
L_s	0.045 nH	0.021 nH	0.051 nH	0.051 nH
TL_1	95 Ω	85 Ω	95 Ω	90 Ω
	0.037 cm	0.037 cm	0.036 cm	0.036 cm
TL_2	98 Ω	85 Ω	95 Ω	110 Ω
	0.035 cm	0.036 cm	0.031 cm	0.04 cm
$C_{t'}$	0.02 pF	0.02 pF	0.02 pF	0.02 pF
g_m	0.059 Siemens	0.034 Siemens	0.044 Siemens	0.045 Siemens
t_d	2 ps	2.2 ps	2 ps	2.1 ps

MATCHING NETWORK SYNTHESIS

One-and two-stage amplifiers were designed using basic microwave thin-film techniques (7). It was important to retain as much of the original device measurement environment as possible, since the equivalent circuit model is a combination of the actual FET S-parameters and the measurement environment. The FET was mounted on top of the substrate and plated through via holes provided ground to the top of the substrate.

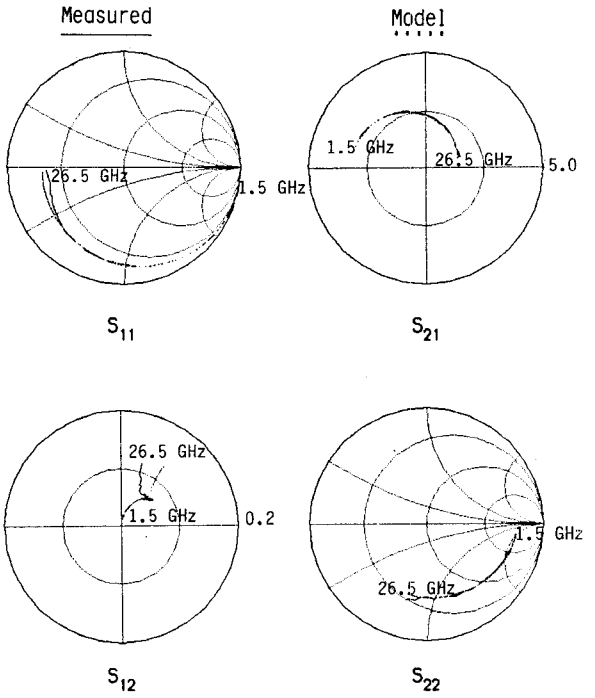

FIGURE 2

Measured and Modeled S-Parameter Comparisons of Device #4

The thin-film matching networks were realized on 5 mil sapphire substrates oriented coplaner orthogonal to the C-axis. Open-and-short-circuted transmission lines were used to realize shunt capacitive and inductive reactances. These along with series, low impedance, quarter wave matching sections were placed at optimum points along the transmission line to obtain maximum gain. The objective was to achieve maximum gain over the required bandwidth and not so much a flat response. Bias was supplied to the devices through 0.7 mil gold bond wires. RF grounds and DC blocking were accomplished with high density chip and thin film capacitors. The circuit dimensions are 5x3.5 millimeters. Coaxial connectors were used on the package. Figure 3 is the equivalent circuit for the one-stage amplifier. The initial computer model predicted a minimum gain of 4 dB from 17-40 GHz (see Figure 4).

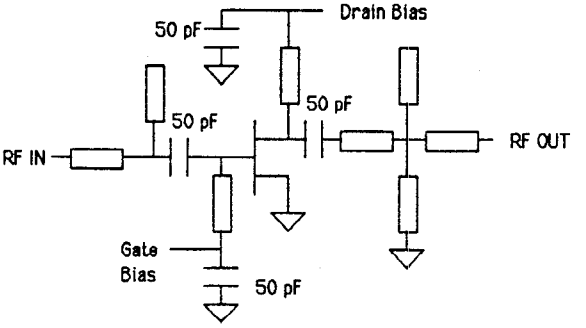

FIGURE 3
One-stage amplifier Equivalent Circuit

AMPLIFIER PERFORMANCE

One and two stage amplifiers were fabricated and tested up to 50 GHz. The amplifier substrates were epoxied on a center-block and sandwiched between two test package end-blocks. The coax connectors and the coax-to-microstrip transitions were part of the end-blocks. Measurements were made on the HP 8510 and the millimeter-wave waveguide based HP 8510 vector network analyzer system. The one-stage amplifier had 1.4 dB minimum gain from 20 - 40 GHz. Lower gain than predicted was due to loss in the test package end-blocks (Fig. 4). The gain ripple was caused by mismatch between the end-blocks and the amplifier input and output impedances. The end-blocks were measured in a through connection without the amplifier. A first approximation equivalent circuit model of the end-blocks was made based on these measured S-parameters. The end-block models tracked the measured through loss data to within +/-0.25 dB. The amplifier computer model was then embedded between the end-block models. This embedded model reduced the difference between the measured and modeled gain to less than +/-1.7 dB from 20-40 GHz (see Fig. 4). Further refinements of the end-block models and microstrip matching element computer models should reduce this difference to less that +/-1 dB. The second harmonic for the single-stage amplifier at 20 GHz and -10 dBm input power was -38 dBc.

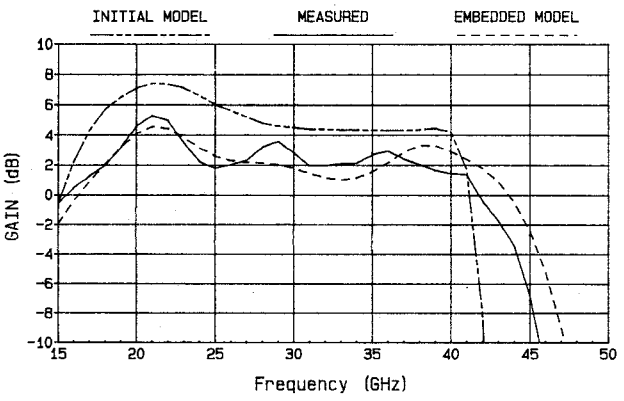

FIGURE 4
Measured and Modeled Gain of One-Stage Amplifier

The input and output reflection coefficients were calculated using the embedded amplifier computer model and compared to the measured results. Figures 5 and 6 are the measured and modeled values of the input and output reflection coefficients respectively. The difference between the measured and modeled phase of the input reflection coefficient was < +/-26 degrees at frequencies between 20 - 35 GHz, and < + 62 degrees from 35 - 40 GHz. The output reflection coefficient showed < +/-38 degrees difference from 20 - 35 GHz, and < + 90 degrees from 35 - 40 GHz. The phase of the input and output reflection coefficients at 40 GHz is significantly affected by small changes in modeling the series line lengths as well as the open stub matching elements.

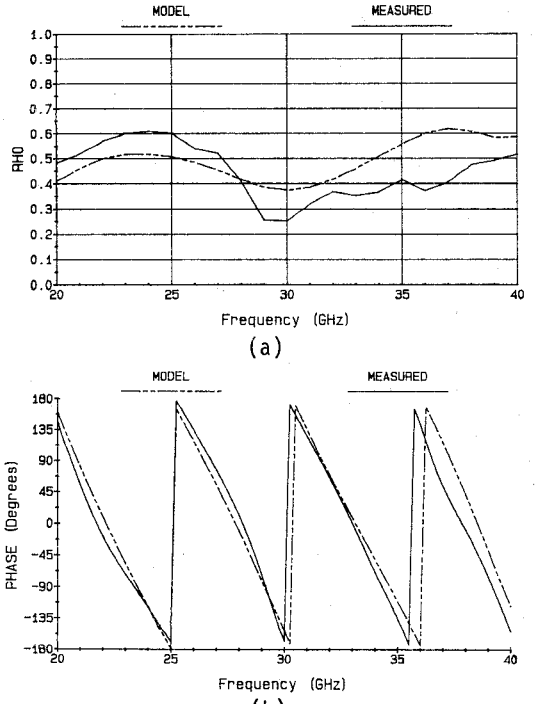

FIGURE 5
(a) Measured vs. Embedded Model of S11 Magnitude
(b) Measured vs. Embedded Model of S11 Phase

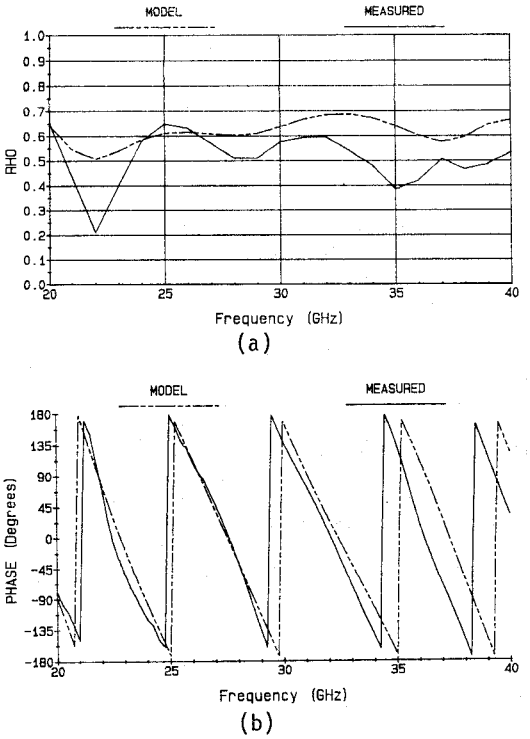

FIGURE 6
(a) Measured vs. Embedded Model of S22 Magnitude
(b) Measured vs. Embedded Model of S22 Phase

The two-stage amplifier performance is shown in Figure 7. Better than 7 dB of gain from 21 GHz to 40 GHz was obtained with low end gain rolloff to 5.5 dB at 20 GHz. This measurement includes the loss in the test package end-blocks. Similar differences to those of the one-stage were observed between the initial two-stage computer modeled gain and the measured gain. At the time of this work, the two-stage had not been embedded between the end-block models, but similar results to those of the one-stage are expected. The second harmonic of the two-stage at 20 GHz with -10 dBm input power was -26 dBc.

The output power of the two-stage amplifier was measured at 30 and 40 GHz. Figure 8 is the output power as a function of the input power at these two frequencies.

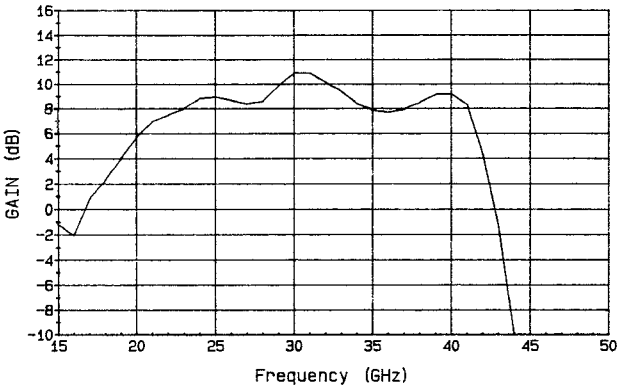

FIGURE 7

Measured gain for the two-stage amplifier

CONCLUSION

We have shown that predicting the performance of millimeter-wave GaAs FET amplifiers can be accomplished by using model-extrapolated S-parameters.

The one stage amplifier measured 1.4 dB minimum gain from 20-40 GHz, 2.8 dB less than the predicted midband gain, because of losses in the test package end-blocks. Embedding the amplifier model between computer models for the end-blocks reduced the difference between the measured and modeled gain for the one-stage to < +/-1.7 dB. Measurement to model error is expected to be reduced to less than +/-1 dB with further improvements in the microstrip models. Second harmonic for the one-stage amplifier with -10 dBm at 20 GHz was -38 dBc.

Measured two-stage amplifier gain was better than 7 dB from 21 - 40 GHz. with low end gain rolloff to 5.5 dB at 20 GHz. Output power at 1 dB gain compression was 8.9 dBm at 40 Ghz and 12.9 dBm at 30 Ghz. Second harmonic with -10 dBm input power at 20 Ghz was -26 dBc.

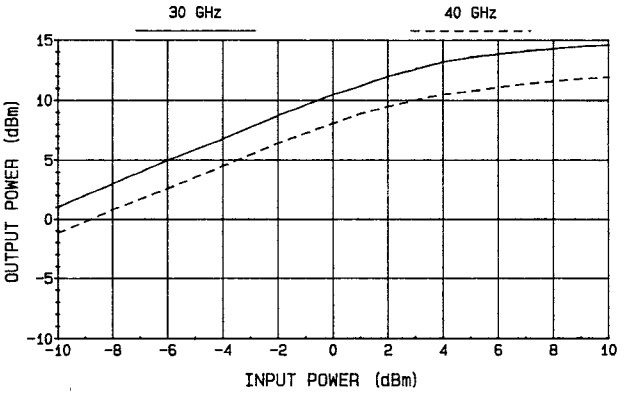

FIGURE 8

Output vs. input power of two stage amplifier

References

(1) J. Rosenberg, P. Chye, C. Huang, and G. Policky, "A 26.5-40 GHz GaAs FET Amplifier," 1982 IEEE MTT-S Digest, pp. 166-168, June. 1983.

(2) E. T. Watkins, J. M. Schellenberg, and H. Yamasaki "A 30 GHz Low Noise FET Amplifier," 1985 IEEE MTT-S Digest, pp. 321-323, June 1985

(3) J. C. Rosenberg, G. J. Policky, and N. K. Osbrinke, "GaAs FET Amplifiers Reach Millimeter Waves," Microwaves, pp. 66-69, 87, June 1982.

(4) E. T. Watkins, J. M. Schellenberg, L. H. Hackett, H. Yamasaki, and M. Feng, "A 60 GHz GaAs Fet Amplifier," 1983 IEEE MTT-S Digest, pp. 145-147, June 1983.

(5) S. Sando, "GaAs FET's Small Gates Yield Big Performance," Microwaves and RF, pp. 141-144, June 1985.

(6) P. W. Chye, and C. Huang, "Quarter Micron Low Noise GaAs FET's," Electron Letters, Vol. 12, pp. 401-403, Dec. 1982.

(7) L. A. Dearden, MS Thesis, Brigham Young University, Provo, Utah, 1986